

REMARKS

Applicants appreciate the Examiner's attention to the above referenced application. Reconsideration of the application is respectfully requested. Claims 55, 38, 41-43 and 45-49 were objected. Claims 1-2, 4-6, 10-17, 20-28, 32-51 and 55-71 were rejected. Claims 3, 7-9, 18-19, 29-31 and 52-54 have been cancelled. Claims 1-2, 4-6, 10-17, 20-28, 32-51 and 55-71 are now pending, of which claims 1, 35, 51, 55 and 67 are independent.

Applicant thanks the Examiner for attention to the claims and their amendments. Accordingly, applicant has checked the claims thoroughly and believes that the current, submitted version of the claims are correct. Therefore, please work from the version of the claims as included above.

Claim Objections

Objections were made to Claims 55, 38, 41-43 and 45-49. Applicant has amended claim 55 to insert the appropriate “of” in line 7.

Claims 38, 41-43, and 45-49 have been amended to consistently reference a “computer readable medium.”

35 USC § 101 Rejection of the Claims

Claims 35-50 were rejected under 35 U.S.C. § 101 because the claimed invention was indicated to be directed to non-statutory subject matter. Applicant has amended claim 35 to a “non-transitory computer readable medium,” according to the Examiner’s suggestion.

35 USC § 102 Rejection of the Claims

Claims 67 and 70-71 were rejected under 35 USC § 102(e) as being anticipated by Kissell (U.S. Patent No. 7,376,954), herein referred to as Kissell. “[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ...” MPEP 706.02 (emphasis added). “The identical invention must be shown *in as complete detail as contained in the ... claim.*” *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920

(Fed. Cir. 1989) (emphasis added). Applicant respectfully traverses this rejection, which should be withdrawn for at least the reasons set forth herein.

Applicant's claim 67 includes, "a third group of resources to be shared by the first shred and the second shred to hold a shared application state, wherein at least a portion of the third group of resources is to be directly updateable by the first and second shred for communication between the first shred and the second shred; wherein the first, second, and third group of resources are private from another privileged-level software entity created thread."

The Office Action alleges that Kissell's disclosure of inter-thread communication storage is equivalent to applicant's third group of resources....to hold a shared application state...and...for communication (See page 6 citing Kissell at col. 16 ll. 37-53). However, Kissell's inter-thread communication is not for private communication between shreds of an OS thread ("third group of resources are private from another privileged-level software entity created thread," and is also not for holding shared application state, as in applicant's claim 67. Instead, Kissell's inter-thread communication allows for synchronizing threads that are executing on different VPEs—independent, physical contexts/processing elements of a processor (see col. 8 lines 10-20)—as illustrated by the disclosure of exposing the address space globally. In other words, Kissell explicitly places the inter-thread communication in a virtual address space (physical memory) instead of context registers to enable communication for synchronization amongst all threads on a processor, while applicant's claim 67 includes a portion of the third group of resources that is both to hold shared application state and be for private communication between privileged-level threads (i.e. communication between first and second shred and the third group of resources being private from another privileged level entity). And as can be seen from the use of the inter-thread communication memory (synchronization for fine grain multithreading from col. 16 ll. 35-53)), Kissell's communication memory is not to hold a shared application state like applicant's claim 67; but instead, it's to hold synchronization information.

35 USC § 103 Rejection of the Claims

Claims 1-2, 4-6, 10-12, 15-17, 20, 22-25, 27-28, 32, 35-44, 47, 50-51, 55-58, 62-65 and 68 were rejected under 35 USC § 103(a) as being unpatentable over Kissell (U.S. Patent No. 7,376,954), herein referred to as Kissell, in view of Hennessy et al.(Non Patent Literature-

“Computer Architecture: A Quantitative Approach”) herein referred to as Hennessy. “The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness.” MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). Applicant respectfully traverses this rejection, which should be withdrawn for at least the reasons set forth herein.

Applicant has amended claims 1, 17, 35, and 51. For example, claim 1 now includes, “wherein the one or more shared registers are private to shreds that share the shared portion of the first application state and the first system state.” And as described above in reference to claim 17, Kissell only discloses inter-thread communication memory that is to enable synchronization between all threads on a processor through use of global access to the physical address space of the inter-thread communication memory. Therefore, there is no disclosure in Kissell that the inter-shred communication memory is to be private amongst shreds sharing a certain state, as in applicant’s claim 1. Moreover, Hennessy is only cited to state that registers are only part of the memory hierarchy, i.e. whatever is done in memory is held in registers. Yet, the allegation of the Office Action (moving Kissell’s inter-thread communication memory to registers) does not render applicant’s claim 1 obvious. In fact, such an allegation would only create registers that hold synchronization information for all threads in a processor, not one or more registers that are private to shreds that share access to the first application state and the first system state, as in applicant’s claim 1.

Applicant notes that claims 17, 35, and 51 have been amended with similar elements.

CONCLUSION

Therefore, applicant respectfully requests reconsideration in view of the remarks and amendments set forth above. If the Examiner has any questions, the Examiner is encouraged to contact the undersigned attorney at 503-712-4988. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0221 and please credit any excess fees to such account.

Respectfully submitted,

Intel Corporation

Customer Number: 59796

Dated: __10/14/2010_____

_____/David P. McAbee/Reg. No. 58,104_____
David P. McAbee
Reg. No. 58,104

Intel Corporation
M/S JF3-147
2111 NE 25th Avenue
Hillsboro, OR 97124
Tele – 503-712-4988
Fax – 503-264-1729